

Reconfigurable Circuits Using Hybrid Hall Effect Devices

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Abstract. Hybrid Hall effect (HHE) devices are a new class of reconfigurable logic devices that incorporate ferromagnetic elements to deliver non-volatile operation. A single HHE device may be configured on a cycle-by-cycle basis to perform any of four different logical computations (OR, AND, NOR, NAND), and will retain its state indefinitely, even if the power supply is removed from the device. In this paper, we introduce the HHE device and describe a number of reconfigurable circuits based on HHE devices, including reconfigurable logic gates and non-volatile table lookup cells.

1 Introduction

Over the last two decades, CMOS circuitry has become the dominant implementation technology for reconfigurable logic devices and semiconductor systems in general, because advances in fabrication processes have delivered geometric rates of improvement in both device density and speed. However, CMOS circuits suffer from the disadvantage that they require power to maintain their state. When power is removed from the system, all information about the state of a computation and the configuration of a reconfigurable circuit is lost, requiring that the reconfigurable device be configured and any information about the ongoing computation be reloaded from non-volatile storage each time the system containing it is powered on.

Magneto-electronic circuits [1] overcome this limitation of CMOS systems by incorporating ferromagnetic materials, similar to those used in conventional hard disks. The magnetization state of these materials remains stable when power is removed from the device, allowing them to retain their state without a power supply and to provide “instant-on” operation when power is restored.

Much of the previous work on magneto-electronic circuits has focused on the use of magneto-electronic devices to implement non-volatile memory. In this paper, we describe a new class of magneto-electronic device, the hybrid Hall effect device [2,4], that can be reconfigured on a cycle-by-cycle basis to implement a variety of logic functions, and present two initial applications for these devices: reconfigurable gates and non-volatile lookup table elements.

In the next section, we describe the HHE device and its basic operation. Section 3 presents two reconfigurable gate designs based on HHE devices, while Section 4 illustrates how the HHE device could be used to provide non-volatile storage for conven-

tional lookup-table based reconfigurable systems. In Section 5, we present simulation results for our circuits. Related work is mentioned in Section 6, and Section 7 presents conclusions and our plans for future work.

2 HHE Device Description and Operation

The hybrid Hall effect device [2] is a semiconductor structure that contains a ferromagnetic element for non-volatile storage. Fig. 1 shows the physical structure of an HHE device along with a functional block diagram. The input to the device is a current along the input wire, which is at the top of Fig. 1(a). As shown in the figure, the current along the input wire creates a magnetic field in the ferromagnetic element beneath it. If the magnitude of the current is high enough, the induced magnetic field in the ferromagnetic element will magnetize it in the direction of the magnetic field, and the magnetization will remain stable once the input current is removed. An input current of sufficient magnitude in the opposite direction will magnetize the ferromagnetic element in the opposite direction, creating two stable states that can be used to encode binary values. If the magnitude of the input current is below the value required to change the magnetization state of the ferromagnetic element, which is a function of the dimensions of the device and the material used to implement the ferromagnetic element, the ferromagnetic element will retain its old magnetization state indefinitely.

The output voltage of the device is generated by passing a bias current through the insulated conductor at the bottom of Fig. 1(a). According to the Hall effect [3], the interaction of this bias current with the magnetic field generated by the magnetized ferromagnetic element produces a voltage perpendicular to the bias current. The sign of this voltage is determined by the magnetization of the ferromagnetic element and its magnitude is proportional to the magnitude of the bias current. Depending on the intended use of the device, a fabrication offset voltage may be added [4], making the output voltage approximately 0V for one magnetization state and VDD for the other.

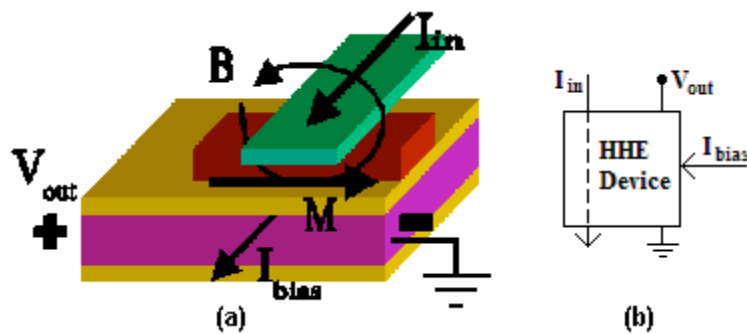


Fig. 1. HHE diagrams. (a) Physical structure. From top to bottom, the blocks represent an input wire, ferromagnetic element, insulator, conducting output channel, and bottom insulator. (b) Functional block.

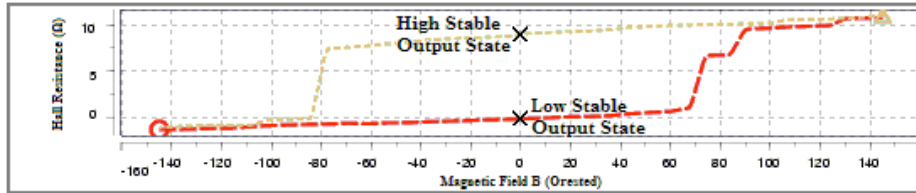


Fig. 2. Hysteresis loop for an HHE device

Adding this fabrication offset makes it significantly easier to integrate the HHE device with CMOS circuits. Previous experiments [4] have fabricated HHE devices a small number of microns on a side, and the technology is expected to scale to significantly smaller devices in the near future, which will also reduce the amount of current required to set the magnetization state of the device.

The behavior of the HHE device is summarized by the hysteresis graph in Fig. 2. The Hall resistance, which relates the magnitude of the output voltage to that of the bias current, is plotted as a function of the magnetic field generated by the current along the input wire. As shown in the figure, there are two stable states when the input current, and thus the magnetic field, is 0, which correspond to the two magnetization states of the ferromagnetic element. A magnetic field of approximately ± 90 Oersted is required to change the magnetization state of the ferromagnetic element and shift the Hall resistance from one half of the hysteresis curve to the other.

3 HHE as a Reconfigurable Gate

Fig. 3 shows a high-level block diagram of the circuitry required to implement a reconfigurable gate using an HHE device. Signals A and B are the inputs to the gate, while signals G0 and G1 select the logic function to be performed by the gate. In the following subsections, we present two designs for the interface circuitry that converts the CMOS-compatible gate inputs into appropriate input currents for the HHE device.

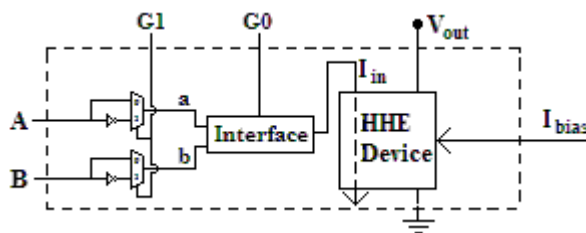


Fig. 3. HHE reconfigurable gate

3.1 HHE Reconfigurable Gate with Reset

Our first reconfigurable gate design uses a reset-evaluate methodology similar to that used in dynamic CMOS circuits. In the reset phase of each clock cycle, an input current of fixed magnitude and direction is applied to the device to set its magnetization state. In the evaluate phase, a current in the opposite direction whose magnitude is determined by the inputs to the reconfigurable gate is applied, possibly switching the magnetization state to the opposite value. An HHE-based gate using this clocking methodology has been demonstrated in [4].

Fig. 4 illustrates the interface logic for a 2-input HHE reconfigurable gate using this methodology. To simplify the interface logic, we assume the use of an HHE gate with two input wires that are vertically stacked in different metal layers. Our conversations with researchers working at the device level indicate that such an extension to the base HHE device is possible, and we are initiating efforts to fabricate a test device with this design.

As shown in the figure, one of the input wires is only used in the reset phase. During this phase, the RESET signal is high, causing a current to flow upward through transistor MR and setting the magnetization state of the HHE device in the direction that corresponds to a logical 0. The PULSE input is held low during this period to ensure that no current flows through the other input wire.

During gate evaluation, the PULSE input is pulled high while the RESET input remains low. Depending on the inputs to the gate, any or all of transistors Ma, Mb, and MG0 may be turned on, allowing a current I_{in1} to flow downward through the input wire. These three transistors are sized such that at least two of them must be on in order for I_{in1} to be large enough to reverse the magnetization state of the HHE device, creating a majority function. Depending on the value of the G0 configuration input, this causes the device to compute either the AND or OR of its other inputs. Similarly, the value of the G1 input shown in Fig. 3 determines whether or not the

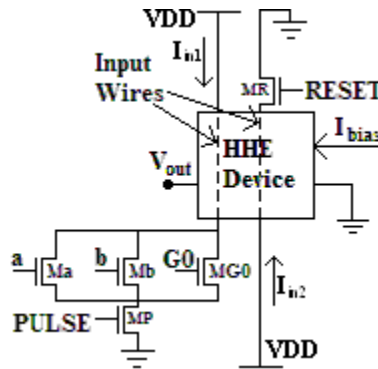


Fig. 4. Interface logic for HHE reconfigurable gate with reset. Current in the left input wire may only flow downwards, while current in the right input wire may only flow upwards.

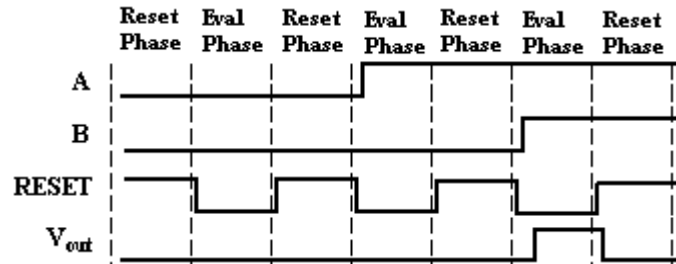


Fig. 5. Waveform of HHE reconfigurable gate operation with reset

inputs to the gate are inverted before they connect to the HHE device, allowing the gate to compute the NAND and NOR of its inputs as well.

Fig. 5 illustrates the operation of the reconfigurable gate when configured to compute the AND of its inputs ($G0 = 0, G1 = 0$). During each reset phase, the magnetization state of the HHE device is configured in the direction that represents a logical 0 by the reset path of the gate. During each evaluation phase, the magnetization state of the gate is conditionally set in the direction that represents a logical 1 based on the value of inputs A and B.

The circuit shown in Fig. 4 can be extended to compute functions of additional inputs by adding additional transistors to the pull-down chain shown in the figure and appropriately sizing the transistors in the pull-down chain. In Section 5, we present simulation results for a four-input reconfigurable gate of the type described in the next subsection. In addition, structures that connect additional configuration inputs in parallel with the transistor MG0 are also possible, allowing the gate to compute threshold or symmetric functions [5,6].

3.2 HHE Reconfigurable Gate with Output Feedback

One drawback to the circuit shown in Fig. 4 is that it consumes power each time the RESET signal is asserted, regardless of the value of its inputs and configuration. If the output of the gate remains constant from one cycle to the next, this can result in significant wasted power. To address this limitation, we have designed the static reconfigurable gate shown in Fig. 6, which uses output feedback to eliminate the need for a reset phase. Rather than resetting the magnetization state of the HHE device to a logical 0 on each cycle, this design provides two conditional pull-down chains, one of which allows current to flow in the direction that sets the device to a logical 0, and one of which allows current to flow in the direction that corresponds to a logical 1. The PULSE input to each pull-down chain prevents static power consumption by only allowing current flow during the time required to evaluate the output of the device. (approximately 2ns for current HHE devices) Feedback from the output of the device to the pull-down chains disables the chain that corresponds to the current output value, preventing power from being consumed on input changes that do not change the output of the device.

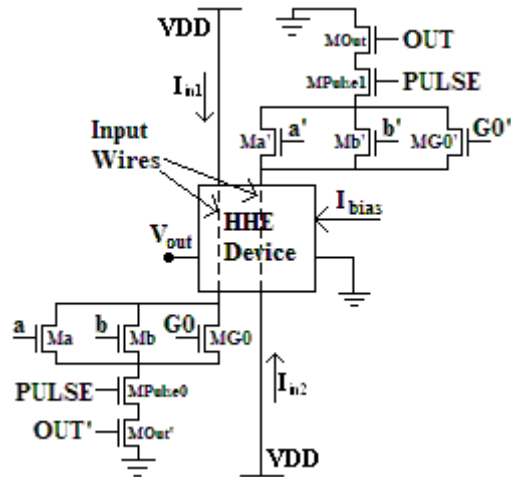


Fig. 6. Interface logic for HHE reconfigurable gate with output feedback

To demonstrate the operation of the gate with output feedback, consider the case where the gate is configured to compute the AND of its inputs ($G_0 = 0$, $G_1 = 0$). In this case, the a and b inputs to the circuit receive the uninverted values of the A and B inputs to the gate, while the a' and b' inputs receive the complement of A and B . Assume that the output of the gate starts at a logical 0. In this case, the left-hand pull-down chain in the figure is enabled, while the right-hand chain is disabled. Since G_0 is set to logical 0, both the A and B inputs to the gate must be high for enough current to flow through the left-hand pull-down chain to flip the magnetization state of the HHE device and change the output of the gate to "1." If the output of the gate starts at a logical 1, however, the right-hand pull-down chain is enabled while the left-hand one is disabled. Because $G_0 = 0$, $G_0' = 1$, and only one of the A or B inputs to the circuit must be 0 for enough current to flow to set the output of the gate to logical 0. Thus, the circuit computes the logical AND of its inputs.

This gate design requires somewhat more configuration logic than the reset-evaluate design, because it is necessary to provide both the true and inverted values of each input signal and the G_0 configuration bit. The set of logic functions that can be computed by this style of gate can be expanded by including configuration circuitry that allows each input to be inverted or disabled individually, reducing the number of gates required to implement a circuit at the cost of increased gate complexity.

HHE reconfigurable gates with input inversion and input enabling may be incorporated into non-volatile reconfigurable logic devices such as PLAs and CPLDs. Currently, EEPROM transistors are the underlying technology of these systems. EEPROMs are useful for realizing product terms with wide-AND operations such as those commonly used in state machines and control logic. HHE-based logic for these devices will be more efficient than EEPROM-based logic because of its greater flexibility. For example, an HHE-based device would allow either two-level AND-OR or

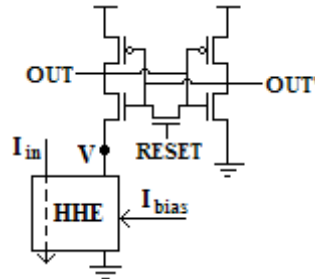


Fig. 7. HHE device incorporated into a logic block LUT cell

two-level OR-AND implementation of a given logical function, depending on which resulted in the fewest number of HHE gates used (i.e. fewest number of product/sum terms.) For complete non-volatile operation, the configuration bits for these HHE gates may be stored in non-volatile HHE LUT cells as described in the next section.

4 Non-volatile LUTs Using HHE Devices

HHE devices may also be used to add non-volatile operation to FPGAs based on more-conventional SRAM lookup tables, as shown in Fig. 7. In this circuit, an HHE device fabricated without an offset voltage is used to store the state of each SRAM cell in a lookup table by applying an appropriate current I_{in} to the HHE device during configuration. The HHE device will retain its state without requiring a power supply, acting as non-volatile storage for the configuration of the device.

To copy the state stored in the HHE device into the lookup table, the RESET signal is asserted to equalize the values of OUT and OUT'. When RESET goes low, a bias current is applied to the HHE device, causing it to generate either a positive or a negative voltage on terminal V depending on the magnetization state of its ferromagnetic element (since the HHE device has been fabricated without an offset voltage.) The cross-coupled inverters in the SRAM cell then act as a differential amplifier, bringing the output voltages of the SRAM cell to full CMOS levels. By applying RESET and the bias current to each SRAM cell in an FPGA simultaneously, the entire device can be reconfigured extremely quickly at power-on.

Although only a single HHE device is depicted in Fig. 7, one more may be added to the right leg of the LUT cell. In this manner, one of two configurations may be dynamically loaded into the LUT cell by applying the appropriate read bias current I_{bias} through the desired HHE device.

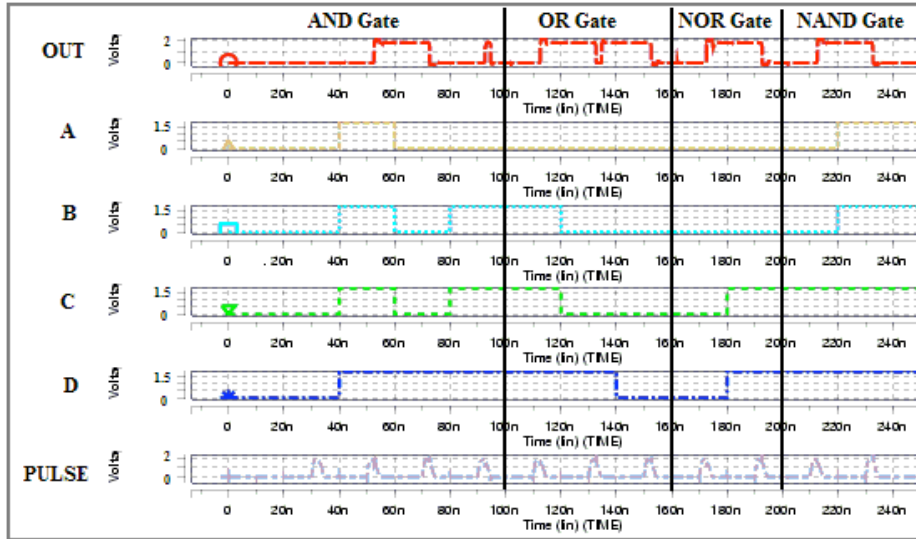


Fig.8. Simulations for HHE reconfigurable gate

5 Simulation Results

Using the HSPICETM circuit simulator, we created a circuit model of the HHE device based on the techniques presented in [7], and have simulated HHE designs for reconfigurable gate structures and non-volatile LUTs. Simulations have also been performed comparing power consumption between a reconfigurable gate with output feedback against one that uses reset pulses. The designs incorporate .18u CMOS transistors in a 1.8V technology.

In Fig. 8, we illustrate the operation of a 4-input HHE reconfigurable gate with output feedback. The gate is configured to compute different functions of its inputs over the course of the simulation, and inputs are allowed to change on multiples of 20ns. 10ns after each input change, the PULSE input to the gate is asserted to cause the gate to compute its output. The simulated device requires 2ns to compute its outputs, matching current experiments with prototype HHE devices.

One may notice that the HHE gate output attempts to switch at 92ns and 132ns. However, the output does not fully switch because not all of the inputs are logic 1 or logic 0 respectively. This indicates that input currents did not exceed the switching threshold of the ferromagnetic element, so the output reverts back to its previous state when PULSE goes low.

Simulations were also performed to compare the power dissipation of a reconfigurable gate using output feedback against one that uses reset pulses. In Fig. 9, we show the input current pulses associated with the input vectors from Fig. 8 for both types

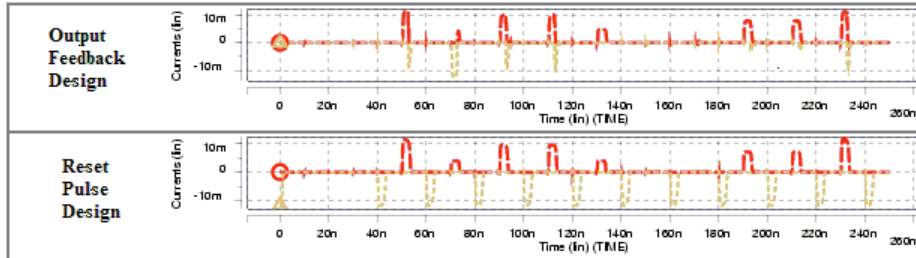


Fig. 9. Input current pulses for output feedback and reset pulse designs for HHE reconfigurable gate. Top curves represent current through left HHE input wire. Bottom curves represent current through right HHE input wire

of gate, illustrating that the reset-based design requires more and larger current pulses than the static gate with output feedback. For these input vectors, simulations show an average power consumption of 4.09mW for the reset pulse design. Average power consumption for the design with output feedback is 1.69mW, an improvement of 2.42x, although power consumption for both gates will scale with clock frequency.

In Fig. 10 we illustrate the operation of a non-volatile LUT using HHE devices. During the first 40ns, the output state of the HHE device is initialized to logic 1 and the RESET signal is high. At 40ns, the RESET signal is removed, and the LUT output becomes the same as that of the HHE device. At 60ns, the power is turned off (VDD=0), and the LUT output decreases exponentially due to discharge effects. At 140ns, power is restored, and the RESET signal is asserted. At 150ns, the RESET signal is disabled, and the LUT output is restored its pre-shutdown value.

6 Related Work

A number of other technologies exist that provide non-volatile storage in reconfigurable devices. Anti-fuses have the benefit of small area, but they are one-time programmable (OTP) and are mainly used for programming interconnections and not logic. EPROMs/EEPROMs are reprogrammable, but consume constant static power since they realize functions using wired-AND logic. Giant-magnetoresistive (GMR) devices are another type of magnetoelectronic device that can easily be integrated into LUT cells [8]. GMR-based designs have the disadvantage that two devices are required

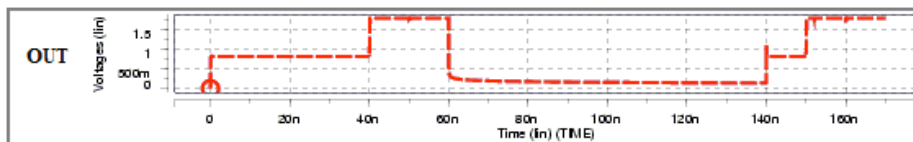


Fig. 10. Simulations for non-volatile LUT using HHE devices

to hold the state of each LUT, as opposed to one HHE device, potentially making them less attractive, although this will depend on how well each type of device scales with fabrication technology.

7 Conclusions & Future Work

Hybrid Hall effect devices are a new class of magnetoelectronic circuit element that can be used to implement non-volatile reconfigurable logic and storage. In this paper, we have presented circuit-level designs for reconfigurable gates and non-volatile lookup table cells based on these devices, demonstrating the potential of these devices. We are currently working with researchers at the Naval Research Lab to fabricate prototypes of these circuits.

Future studies of HHE-based reconfigurable logic will focus on the system issues involved in building large-scale reconfigurable logic systems based on magnetoelectronic devices. In particular, the small size and fine-grained reconfigurability of these devices makes them very attractive and is leading us towards the design of systems based on simple logic blocks and regular interconnect patterns, trading reduced logic block utilization for reductions in interconnect area and complexity.

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